rejected under 35 U.S.C. 103(a) as being unpatentable over Zscheile et al. in view of Kartchner et al. (US 4638494) or Abrahamson et al. (5022049). Claims 22 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Zscheile Jr. et al. in view of Keller (US 7,321,609). Claims 9, 11, 13-18 and 24 are allowed over prior art of record. Claim 5 was objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

The Examiner is requested to reconsider the rejected claims in light of the reasoning presented below. A separate sheet showing the status of all claims, in accordance with C.F.R. 121 is enclosed.

First, the Applicants respectfully point out that Zscheile's delays have nothing to do with the PN phase delays as in the present invention and are merely Zscheile's method to prevent a potential undesirable combination outcome, i.e., cancellation. Stated differently, if Zscheile did not delay his component codes then the likely outcome is cancellation when combining the component codes with Zscheile's non-linear composite code. Thus, Zscheile's delays are merely a safeguard and have nothing to do with PN phase delays.

PN phase delays in the present invention are achieved by delaying one COMPONENT code (by one or more chips) relative to the other non-delayed (or differently delayed) COMPONENT codes, prior to being combinatorially combined; the phase of the COMPOSITE PN code slips or advances by a deterministic number of chips "substantially equal to at least one combination epoch of the relatively prime PN component codes

not slipped." Simply stated, slip one code by one or more chips relative to the phase of its companion component codes, and a deterministic slip or advance occurs in the resulting composite PN code. The phase slip is deterministically millions or billions of chips. In claim 1 this is recited as, "wherein each of the plurality of composite PN codes are separated by a predetermined PN phase" [Emphasis added].

Because the slipped PN code is millions or billions of chips separated in phase from the un-slipped version of the PN code, the two PN sequences do not correlate and are so far separated in phase that they do not correlate even during acquisition when the phase uncertainty of each of the codes is much less than millions or billions of chips, which means that there is no worry of correlation or interference during periods of phase uncertainty. Thus, in the present invention a single PN code generator can create many uncorrelated codes by delaying one of the component codes by one or more chips. This is referred to as Phase Division Multiple Access (PDMA) in the present invention.

As pointed out earlier, Zscheile merely delays component codes so that the codes are not "cancelled" when combined with Zscheile's non-linear derivative composite code Z:

> "Preferably, the codes, C 1 , C 2 , . . . C n -1, when applied to combiners 20, 22 are time delayed relative to these same codes incorporated by the nonlinear composite code Z. Such time delay for codes, C 1 , C 2 , . . . C n -1, may be brought

about by delays 58, 60, 62. The purpose for the time delay is so that the portions of the component codes, C 1 , C 2 , . . . C n -1, incorporated in the nonlinear composite code Z will not be canceled out by the MAJ and MOD combining of the code Z with these same component codes. [Zscheile, col. 9, lines 1-11]

Thus, Zscheile does not disclose or suggest delaying component codes by a predetermined "PN phase" in a Phase Division Multiple Access (PDMA) as in the present invention. Indeed, nowhere does Zscheile even mention the term "Phase Division".

In the claim by claim analysis below it will be shown that the present application claims features not otherwise disclosed or suggested by the prior art.

102(b) rejections

Claims 1-3, 7-8, 22, and 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Zscheile, Jr. et al (US 4,225,935).

Claim 1 of the present application recites the features of a receiver logic combiner adapted to generate a plurality of *relatively prime composite PN codes*, wherein *each* of the plurality of composite PN codes *are separated by a predetermined PN phase.*

As pointed out above and repeated here, Claim 1 of the present application also recites the feature of the *composite* PN codes are *separated by a predetermined PN phase.*

It will be appreciated that the present application delays the output of one PN component code by 0, 1, 2, 3, or n chips. When this n-delayed component code is combinatorially combined with other relatively prime component codes, the composite code is deterministically shifted as a function of the n-number of chip delays. This means that the phase difference is deterministic between the composite PN code with n=0 delay and the otherwise same composite PN code with n not-equal-to-zero delay. The deterministic composite code phase shift is millions or billions of chips, but the phase shift is deterministic to the chip. Thus, the deterministic composite code phase shift is not one PN minor epoch, it is "a phase offset in the composite code equal to at least one combination epoch of the [component] codes not slipped. The composite code slip is a number (many) times the lengths of the component codes not experiencing the one or more chip delay relative to the other component codes.' It will be appreciated that with the delay of one component code by n chips, the composite PN code sequence is advanced in phase by millions or billions of chips, the exact number of which is perfectly known. This provides an immediate and effectively new code. Not only is the new code orthogonal to the unslipped version of itself, it is separated in phase from the unslipped version of itself by millions or billions of chips, far beyond any uncertainty that can be practically searched. The above features are readily

claimed in pending claims 1-4, 9-11, 22, and 23. For example, claim 1 of the present application recites the features:

> "...at least one receiver logic combiner adapted to generate a plurality of relatively prime composite PN codes, wherein each of the plurality of composite PN codes are separated by a predetermined PN phase."

This feature is not disclosed or suggested in Zscheile.

As pointed out earlier, Zscheile never says anything about phase shifts or phase divisior. Zscheile informs that what he is doing with his delays (column 9, lines 6-11), "The purpose for the time delay is so that the portions of the component codes, C1, C2, . . . CN-1, incorporated in the nonlinear composite code Z will not be canceled out by the MAJ and MOD combining of the code Z with these same component codes."

Zscheile splits his code to two different paths, and the two paths meet again at the combinatorial (MAJ and MOD) combiners. If the codes from the two paths meet up at the combiners with the same phase, the codes cancel. Zscheile does not want them to cancel, so Zscheile puts a delay in one of the paths.

It should also be noted that Zscheile does not disclose or suggest if all of Zscheile's delays are the same or different; only that the delays are used to avoid cancellation. Thus, for at least this reason, Zscheile teaches contrary to the teachings of the present invention in that Zscheile delays his linear codes relative to his non-linear code so that the linear codes do not cancel at the combiners. The present

invention, on the other hand, specifically claims that the phases of the component codes must be different in order to achieve the phase division (deterministic phase shift), i.e., predetermined PN phase.

Claim 22 of the present application recites the feature of a program of instructions executable by the machine to perform method steps for generating multi-phase composite pseudo-noise (PN) codes. In addition, Claim 22 recites the features of generating a plurality of relatively prime PN component codes and combining the plurality of relatively prime PN component codes to generate a composite PN code. Claim 22 also recites the feature of generating a second plurality of relatively prime PN component codes, wherein one of the component codes is PN phase delayed, and combining the plurality of relatively prime PN component codes to generate a second composite PN code. The result is that the second composite PN code is phased delayed by a deterministic delay substantially equal to at least one combination epoch of the component codes not slipped. Nowhere does Zscheile disclose or suggest phase delaying a component code by a predetermined phase delay, i.e., PN phase delay, to form a second composite PN code phased delayed where the phase delay is substantially equal to at least one combination epoch of component codes not slipped.

Claim 23 of the present application recites a program storage device having at least one Very High Speed Integrated Circuit (VHSIC) Hardware Description (VHDL) Language file. Nowhere does Zscheile disclose or suggest VHDL language files.

Therefore, in light of the above, Claims 1-3, 7-8, 22, and 23 are patentable and should be allowed.

103(a) rejections

Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Zscheile, Jr. et al. Claims 6-8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Zscheile et al. in view of Kartchner et al. (US 4638494) or Abrahamson et al. (5022049). Claims 22 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Zscheile Jr. et al. in view of Keller (US 7,321,609).

Dependent claim 4 rises or falls with independent claim 1.

Dependent claims 6-8, all recite the features of MAND, MAJ, or MOD logic combination of the relatively prime PN codes. As pointed out earlier and repeated here Zscheile fails to disclose or suggest the parent claim features of *predetermined phase separation between relatively prime composite codes* from which these claims depend. In addition, neither does Kartchner et al., or Abrahamsom et al., disclose or suggest MAND, MAJ, or MOD logic combination of the relatively prime PN codes where one of the combination codes has been PN phased delayed by a predetermined amount.

Therefore claims 6-8 are patentable and should be allowed.

Regarding claims 22 and 23, the Examiner is directed to MPEP 35 U.S.C 103 (c):

> (1) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of **section 102** of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person.

In this instance, both the present application and the prior art reference Keller, cited by the Examiner are assigned to the same entity. Therefore, under 35 U.S.C. 103 (c) the Keller prior reference is not valid. Thus, claims 22 and 23 are patentable and should be allowed.

Allowable Claims

Claims 9, 11, 13-18 and 24 are allowed over prior art of record. Claim 5 was objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

The Applicants respectfully assert that all of the pending claims are now in a condition for allowance.

Should any unresolved issue remain, the Examiner is invited to call Applicant's Attorney at the telephone number indicated below.

Respectfully submitted,

/Kevin P. Correll/ December 1, 2008

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